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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,954	08/04/2005	Jean-Luc Pamart	BDM-05-1139	1017
35811 7590 07/13/2010 IP GROUP OF DLA PIPER LLP (US) ONE LIBERTY PLACE 1650 MARKET ST, SUITE 4900 PHILADELPHIA, PA 19103			EXAMINER WANG, QUAN ZHEN	
			ART UNIT 2613	PAPER NUMBER
			NOTIFICATION DATE 07/13/2010	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pto.phil@dlapiper.com

Office Action Summary

Application No.

10/536,954

Applicant(s)

PAMART ET AL.

Examiner

QUAN-ZHEN WANG

Art Unit

2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24-38 and 40-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24-38 and 40-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/GS/US)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/23/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 24-32 and 38-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis (U.S. Patent US 5,953,138) in view of Wolf (U.S. Patent Application Publication US 2001/0038475 A1).

Regarding **claims 24 and 38**, Ellis teaches an apparatus (figs. 1 and 7) for transmitting data on an optical fiber, comprising:

a plurality of monochrome transmitters, each of which has its own transmission wavelength and inherently having a local clock,

a multiplexer (figs. 1, multiplexer 105 and fig. 7 multiplexer 740);
an optical gate that comprises a clock and that receives multiplexed NRZ format signals and cutting signal produced by a master clock, and that reformats said multiplexed NRZ formatted signals to multiplexed RZ signals (figs. 1 and 7); and
a master clock controlling the clock of the optical gates.

Ellis differs from the claimed invention in that Ellis does not specifically disclose that the local clocks are slave clock being controlled by the master clock. However, utilizing master-slave technique in optical communications is well known. for example, Wolf discloses each of the optical transmitters in a system having a slave local clock (paragraph 3 teaches a slave clock in lower level network elements), wherein each slave local clock from each transmitter is controlled by a synchronization circuit comprising a master clock and a phase locked loop (PLL) (paragraph 3 teaches a master clock for synchronizing slave clocks and paragraph 22 teaches a phase-locked loop as a method for synchronizing signals), said master clock controlling the clock of each slave local clock by using said phase locked loop which supplies the synchronization signal for each of the transmitters (paragraph 3 teaches the master clock and paragraph 22 teaches the PLL for synchronization purposes).

Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to incorporate the master-slave technique of Wolf in the system of Ellis. The motivation would have been to synchronize the optical gate with signals of the transmitters.

Regarding **claim 25**, Ellis further discloses reformatting the data is common and simultaneous for all carriers (figs. 1-7).

Regarding **claims 26-27**, Ellis further discloses optimizing the form of the signal as a function of characteristics of propagation of an associated transport means, and optimizing optical parameters of the signal as a function of the characteristics of propagation of an associated transport means (figs. 3-6).

Regarding **claim 28**, Ellis further discloses stabilizing temporal parameter of data (fig. 5).

Regarding **claim 29**, Wolf further teaches a process comprising synchronizing streams (pulses) emitted by the transmitters (paragraph 5 teaches synchronization signals for synchronizing the data emitted by the transmitters).

Regarding **claim 30**, Wolf further teaches a process wherein the formatting comprises aligning the phase of signals generated by the transmitters (paragraph 22 teaches a phase locked loop that locks and aligns the phases).

Regarding **claim 31**, Wolf further teaches a process wherein the aligning is subject to ambient parameters to compensate for temporal signal variations (paragraph 22 teaches the signals being synchronized with the synchronization signals after transmission through a network that inherently includes ambient parameters).

Regarding **claim 32**, Wolf further teaches a process wherein the aligning is subject to ambient parameters to compensate for differences and variations between optical paths (paragraph 11 teaches different optical paths for the signals and paragraph 22 teaches the signals being synchronized with the synchronization signals

after transmission through a network that inherently includes ambient parameters and explicitly includes different optical paths).

4. **Claims 33-37 and 40-44, and 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis (U.S. Patent US 5,953,138) in view of Wolf (U.S. Patent Application Publication US 2001/0038475 A1), and further in view of Mussino (U.S. Patent US 5,812,297).

Regarding **claim 33**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differs from the claimed invention in that they do not teach an embodiment wherein each element of the multiplexer is signed before multiplexing by a frequency marker applied on the phase. However, it is known in the art to use frequency markers applied on the phase. For example, Mussino teaches applying a frequency marker to a phase before transmitting (column 8, lines 13-17 teach phase modulating a pilot tone, which is equivalent to a frequency marker applied on the phase, and figure 1, items 6 and 7 teach the modulation as being applied before the signal enters any network or multiplexer). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Ellis and Wolf with the teaching of Mussino for encoding information about bias voltage, or possibly another physical system value, onto a pilot tone in an optical signal (column 2, lines 59-67 teach this advantage).

Regarding **claim 34**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differs from the claimed invention in that they do not teach an

embodiment wherein each element of the multiplexer is signed before multiplexing by a frequency marker applied on the phase. However, Mussino teaches applying a frequency marker to an optical signal's amplitude before multiplexing (column 8, lines 13-17 teach amplitude modulating a pilot tone, which is equivalent to a frequency marker applied on the phase, and figure 1, items 6 and 7 teach the modulation as being applied before the signal enters any network or multiplexer). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Ellis and Wolf with the teaching of Mussino for encoding information about bias voltage on a pilot tone in an optical signal (column 2, lines 59-67 teach this advantage).

Regarding **claim 35**, Mussino further teaches a process where the marker comprises a signal with a predetermined spectrum (column 2, lines 60-61 teach the pilot tone having a predetermined frequency, or spectrum).

Regarding **claim 36**, Mussino further teaches a process where the marker comprises a signal with a spectrum whose characteristics are a function of the disturbances undergone by the signal on a corresponding path (column 3, lines 20-25 teach looking for the presence of disturbances based on the pilot signals).

Regarding **claim 37**, Mussino further teaches the process where characteristics of the marker are determined to disturb a marked signal in such a manner that marking is evanescent during passage through the gate (column 8, lines 27-36 teach attenuating the pilot tone by adding it with a phase shifted version of itself as it propagates through the gate).

Regarding **claim 40**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differs from the claimed invention in that they do not teach an apparatus further comprising frequency marking circuits for each element of the multiplex. However, Mussino teaches a frequency marking circuit for a transmitter (column 8, lines 48-53 teach a quartz oscillator element for generating pilot tones for imposing a lower-frequency modulation on a signal prior to entering a network or Application/Control Number: 10/536,954 Page 12 Art Unit: 2613 multiplexer, wherein the oscillator is inherently part of a circuit requiring an active power source). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Ellis and Wolf with the teaching of Mussino for encoding information about bias voltage, or possibly another physical system value, onto a pilot tone in an optical signal (column 2, lines 59-67 teach this advantage).

Regarding **claim 41**, Mussino further teaches the frequency marking circuit applying the marking signal onto a transmitter (column 8, lines 55-57 teach the marking signal being applied to the modulator of a transmitter). Ellis, Wolf and Mussino do not teach a plurality of frequency marking circuits and transmitters. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use multiple circuits for the multiple transmitters of Wolf's embodiment (paragraph 19 teaches the plurality of signals being transmitted from multiple transmitters) since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding **claim 42**, Mussino teaches applying a frequency marker to a phase before transmitting (column 8, lines 13- 17 teach a frequency marking via phase of a pilot tone, which is equivalent to a frequency marker applied on the phase, and figure 1, items 6 and 7 teach the modulation as being applied before the signal enters any network or multiplexer).

Regarding **claim 43**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differ from the claimed invention in that they do not teach an apparatus wherein the optical gate comprises a detector for each marker to control characteristic of the formatting and adjustment of the phase of a corresponding path. Mussino teaches applying a frequency marker to a phase before transmitting (column 8, lines 13-17 teach a frequency marking via phase of a pilot tone, which is equivalent to a frequency marker applied on the phase, and figure 1, items 6 and 7 teach the modulation as being applied before the signal enters any network or multiplexer). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Ellis and Wolf with the teaching of Mussino for encoding information about bias voltage, or possibly another physical system value, onto a pilot tone in an optical signal (column 2, lines 59- 67 teach this advantage).

Regarding **claim 44**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differ from the claimed invention in that they do not teach an apparatus wherein the optical gage comprises a spectral analyzer for the marker to adjust the phase of each path. Mussino teaches a spectral analyzer for the marker to

adjust the phase of each path (column 4, lines 5-8 teach a linearizer circuit that adjusts the frequency-dependent input into a pre-determined output, inherently performing a spectral analysis and system response to the signal, and column 5, lines 16-21 teach the linearizer circuit adjusting the phase of the frequency- marking pilot signal). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Ellis and Wolf with the teaching of Mussino for predistorting signals to reduce distortions in transmission (column 2, lines 37-45 teach this advantage).

Regarding **claim 46**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Ellis and Wolf differ from the claimed invention in that they do not teach that the system includes a counter-reaction circuit for the communication system that generates a frequency marker. Mussino teaches a counter-reaction circuit for an apparatus that transmits data on an optical fiber and which generates a frequency marker (column 2, lines 59-67 teach applying a sinusoidal pilot tone signal, or frequency marker) for injecting a disturbing spectral signal of a transmitter comprising a detector (column 2, line 63 teaches the detector) for an output signal of a gate that acts on an automatic controller of a transmitter phase that obtains a selected spectral transformation of each marker (column 5, lines 16-21 teach a linearizer circuit which receives a spectral signal as an input and automatically performs operations according to predetermined values to operate on the phase).

5. **Claim 45** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis (U.S. Patent US 5,953,138) in view of Wolf (U.S. Patent Application Publication US 2001/0038475 A1), and further in view of Nishihara (U.S. Patent US 6,512,616 B1).

Regarding **claim 45**, Ellis and Wolf have been discussed in regard with claims 24 and 38. Wolf further teaches a demultiplexer (paragraph 20 teaches a demultiplexer). However, Ellis and Wolf do not teach an optical converter and a clock connected to at least one of the converters. Nishihara teaches an optical converter and a clock connected to the converter (column 7, lines 23-30 teach the conversion of a clock signal to an optical transmission). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Ellis and Wolf with the teaching of Nishihara for performing packet switching in an optical network wherein the retiming of packet data in the output section is facilitated and an increase in the scale of the circuitry is suppressed (column 4, lines 31-37 teach this advantage). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Ellis and Wolf with the teaching of Mussino for encoding information about bias voltage on a pilot tone in an optical signal (column 2, lines 59-67 teach this advantage).

Response to Arguments

6. Applicant's arguments filed on 6/23/2010 have been fully considered but they are not persuasive.

Regarding claim 24, Applicant recognizes that Ellis discloses a system for converting NRZ formatted signals into RZ formatted signals. That system includes a plurality of monochrome transmitters, each of which has its own transmission wavelength, a coupler that may be assimilated to a multiplexer and an optical gate that receives multiplexed NRZ formatted signals which then converts those signals into multiplexed RZ formatted signals. Applicant also recognizes that each of the monochrome transmitters includes an internal clock. Applicant argues that Ellis does not disclose a synchronization circuit comprising a master clock and a phase locked loop that controls the clock of the transmitters and the clock of the optical gate and Wolf is different from Ellis and one skilled in the art would not combined Wolf with Ellis.

However, any ordinary skilled in the art would understand that in order to convert the multiplexed NRZ signal into RZ signal, the clock of the optical gate and the clock of the transmitters have to be synchronized. If the clocks were not synchronized, the system of Ellis simply would not work. That is to say the clock synchronization is inherent in Ellis even though Ellis does not specifically disclose how the clocks are synchronized.

While, prior art reference Wolf discloses a method to synchronize clocks. Specifically, Wolf discloses each of the optical transmitters in a system having a slave local clock (paragraph 3 teaches a slave clock in lower level network elements), wherein each slave local clock from each transmitter is controlled by a synchronization circuit comprising a master clock and a phase locked loop (PLL) (paragraph 3 teaches a master clock for synchronizing slave clocks and paragraph 22 teaches a phase-locked

loop as a method for synchronizing signals), said master clock controlling the clock of each slave local clock by using said phase locked loop which supplies the synchronization signal for each of the transmitters (paragraph 3 teaches the master clock and paragraph 22 teaches the PLL for synchronization purposes).

In accordance with KSR, "It is common sense that familiar items may have obvious uses **beyond their primary purposes**, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle." See KSR, 137 S. Ct. at 1742, 82 USPQ2d at 1397. For the instant case, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to incorporate the master-slave technique of Wolf in the system of Ellis in order to synchronize the optical gate with signals of the transmitters.

For the above reasons, the rejections still stand.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN-ZHEN WANG whose telephone number is (571) 272-3114. The examiner can normally be reached on 9:00 AM - 5:00 PM, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

7/6//2010
/Quan-Zhen Wang/
Primary Examiner, Art Unit 2613